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Question Paper Code : 80335

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Electronics and Communication Engineering

EC 6304 – ELECTRONIC CIRCUITS - I

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

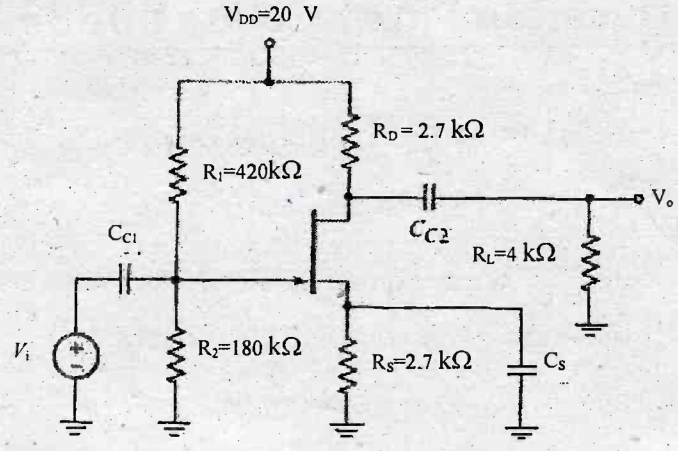
1. What is a Q point?
2. What is the impact of temperature on drain current of MOSFET?
3. What is an ac load line?
4. Draw the small-signal ac equivalent circuit of the BJT.
5. What is the impact of including a source resistor in the FET amplifier?
6. Why multi-stage amplifiers are required?
7. What is the reason for reduction in gain at lower and higher frequencies in case of amplifiers?
8. Determine the unity-gain bandwidth of a FET with parameters, Cgd = 10 fF, Cgs = 50 fF and g_m = 1.2 mA/V.
9. Why active loads are not used with discrete circuits?
10. Define CMRR.

PART B — (5 × 13 = 65 marks)

11. (a) Analyze a BJT with a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be $R_{B1} = 56\,k\Omega$, R_{B2}=12.2 kΩ, R_C= 2 KΩ, R_E = 0.4 kΩ, V_{CC} = 10 V, $V_{BE}(on)$ = 0.7 V, and β =100.

Or

(b) Consider the circuit shown below with transistor parameters I_{DSS}=12 mA, V_P = –4V, and λ = 0.008 V^{-1}. Determine the small-signal voltage gain A_v = vo/vi.

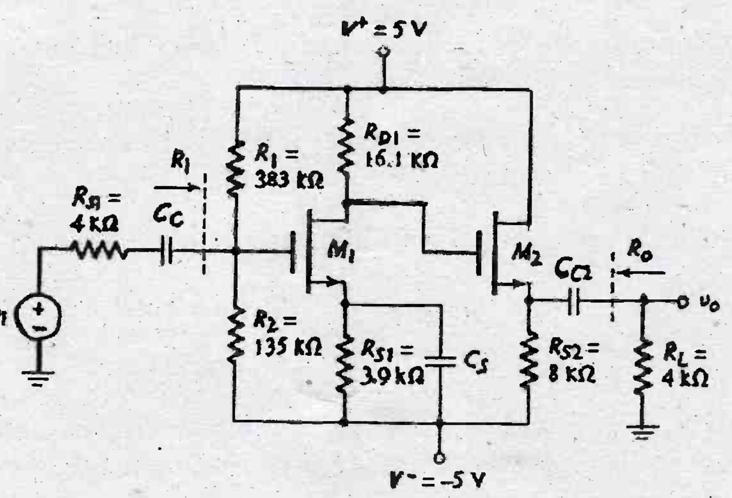


12. (a) Analyze a basic common-base amplifier circuit and derive the expressions for its small-signal voltage gain, current gain, input impedance and output impedance.

Or

(b) With neat diagrams, explain the operation and advantages of Darlington pair circuit. Also analyze its small-signal voltage gain and input impedance.

13. (a) Determine the small-signal voltage gain of a multistage cascade circuit shown in the figure below. The transistor parameters are K_{n1} = 0.5 mA/V², K_{n2} = 0.2 mA/V², $V_{TN1}=V_{TN2}$=1.2 V and $\lambda_1 = \lambda_2$ = 0. The quiescent drain currents are I_{D1} = 0. 2 mA and I_{D2} = 0.5 mA.



Or

(b) (i) Draw the circuit of a basic common source amplifier with voltage divider bias and derive the expressions for voltage gain, input impedance and output impedance using small-signal model. (8)

(ii) Determine the voltage gain of the circuit, assuming the following parameters: V_{DD} = 3.3 V, R_D= 10 kΩ, R_{G1}= 140 kΩ, R_{G2} = 60 kΩ, and R_{Si} = 4 kΩ. The transistor parameters are: V_{TN} = 0.4 V, K_n = 0.5 mA/V², and $\lambda = 0.02\ V^{-1}$. (5)

14. (a) Derive the expression for cut-off frequency of a BJT.

Or

(b) Construct the high frequency equivalent circuit of a MOSFET from its geometry and derive the expression for short circuit current gain in the common-source configuration.

15. (a) Draw and explain the operation of a simple MOSFET amplifier with active load and derive its voltage gain using small-signal equivalent circuit.

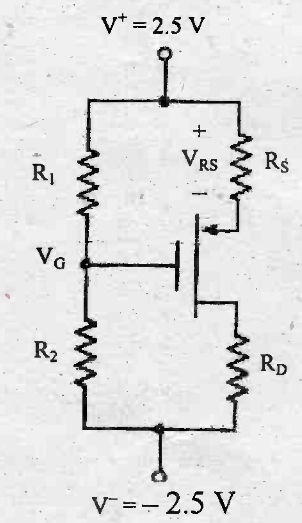
Or

(b) With necessary diagrams, explain the operation of a CMOS differential amplifier. Using small signal analysis, derive the expression for its voltage gain.

PART C — (1 × 15 = 15 marks)

(Application/Design/Analysis/Evaluation/Creativity/Case study)

16. (a) Design the circuit given below such that $I_{DQ} = 100\ \mu A$, $V_{SDQ} = 3V$, and $V_{RS} = 0.8\,V$. Note that V_{RS} is the voltage across the source resistor R_S. The value of the larger bias resistor, either R_1 or R_2 is to be 200 $k\Omega$. Transistor parameter values are $Kp = 100\ \mu A / V^2$ and $V_{TP} = -0.4\,V$. The conduction parameter, Kp may vary by ±5 percent.



Or

(b) Design the cascode circuit shown below to meet the following specifications: $V_{CE1} = V_{CE2} = 2.5\,V, V_{RE} = 0.7\,V, I_{C1} \cong I_{C2} \cong 1\,mA,$ and $I_{R1} \cong I_{R2} \cong I_{R3} = 0.10\,mA$.